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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/788,582	02/16/2001	John Susantha Fernando	9-11-4	8752

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EXAMINER	
CHANDRASEKHAR, PRANAV	
ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 12/23/2003 5

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/788,582	FERNANDO ET AL.	
	Examiner	Art Unit	
	Pranav Chandrasekhar	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1,2,6,8,11,14-17 and 21-23 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kanuma [US Pat No. 4,587,445].

2. As per claim 1, Kanuma teaches a method for transmitting a control signal on a bus, which comprises:

transferring a first signal state [data value equal to 1] of the control signal by adjusting a voltage level from a previous time interval. [Fig. 2; col. 3 lines 33-68;col. 4 lines 1-3. The voltage level of data values 0 and 1 are VL and VH respectively. When the data value changes from 0 to 1, the voltage is adjusted from VL to VH, col. 5 lines 25-26.];

transferring a second signal state [data value equal to 0] by maintaining said voltage level from the previous time interval. [Fig 2; col. 4 lines 5-48. When the data value changes from 0 to 0, the voltage is maintained at VL from the previous time interval, col. 5 lines 25-26].

3. As per claim 8, Kanuma teaches a method for receiving a control signal that comprises:

detecting a first signal state for said control signal if a voltage level from a previous time interval is adjusted; [28-1 – 28-N Fig 2; col. 3 lines 37-51]

detecting a second signal state if said voltage level from the previous time interval is maintained. [28-1 – 28-N Fig 2; col. 3 lines 42-46; col. 3 lines 52-58]

4. As per claim 16, Kanuma teaches a device for communicating a control signal having two signal states on a communication bus,that comprises

a memory element for maintaining a voltage level from a previous time interval; [22-1 – 22-N Fig 2; col. 3 lines 33-61; col. 4 lines 15-20. Based on the cited lines, it is evident that a D Flip-Flop maintains the voltage level from a previous time interval.]

a comparison circuit for detecting a change in said voltage level from the previous time interval [28-1 – 28-N Fig 2; col. 2 lines 62-65; col. 3 lines 33-61;col. 4 lines 15-20] indicating an assertion of control signal by another device. [col. 1 lines 14-17. The logic generating the control signals T1-TN is interpreted to be another device.]

an adjustment circuit for changing said voltage level from the previous time interval [20-1 – 20-N Fig 2; col. 3 lines 37-51;col. 4 lines 28-31] indicating an assertion of control signal by another device. [col. 1 lines 14-17. The logic generating the control signals T1-TN is interpreted to be another device.]

5. As per claims 2, 11, and 17, Kanuma teaches the step of maintaining the voltage level from the previous time interval using a memory element. [22-1 – 22-N Fig 2; col. 3 lines 33-61; col. 4 lines 15-20. Based on the cited lines, it is evident that a D Flip-Flop maintains the voltage level of the previous time interval.]

6. As per claims 6,14 and 21, Kanuma teaches the step of transitioning from a first voltage level VL [corresponding to a data value 0], to a second voltage level VH [corresponding to a data value 1]. [col. 3 lines 33-68; col. 4 lines 1-3].

7. As per claim 15, Kanuma teaches a step of applying received control signal state to an exclusive-OR gate with voltage level from the previous time interval to determine the signal level to be asserted in the current time interval. [28-1 – 28-N Fig 2; col. 3 lines 42-58].

8. As per claim 22, Kanuma teaches a device wherein the adjustment circuit is an exclusive-OR gate. [20-1 – 20-N Fig 2; col. 3 lines 37-51]

9. As per claim 23, Kanuma teaches a device wherein the comparison circuit is an exclusive-OR gate. [28-1 – 28-N Fig 2; col. 2 lines 62-65; col. 3 lines 33-61;col. 4 lines 15-20]

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanuma [US Pat No. 4,587,445] in view of Azarya et al [US Pat No. 5,978,578].

Kanuma does not explicitly teach the step of ensuring that only a single node connected to the bus can assert a control signal in a given time interval.

Azarya teaches the step of ensuring that only a single node connected to the bus can assert a control signal in a given time interval [col. 13 lines 54-56] in order to reduce cross-talk between adjacent control signals.

11. Claims 4,5,7,12,13,19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanuma [US Pat No. 4,587,445].

12. As per claims 4,12 and 19, Kanuma does not explicitly teach the bus being on a system-on-chip (SoC).

It would have been obvious to one skilled in the art that the data output circuit (comprising bus lines) taught by Kanuma may be implemented on a system-on-chip (SoC).

13. As per claims 5,13 and 20, Kanuma does not explicitly teach the bus being on a printed circuit board (PCB).

It would have been obvious to one skilled in the art that the data output circuit (comprising bus lines) taught by Kanuma may be implemented on a printed circuit board (PCB).

14. As per claim 7, Kanuma does not explicitly teach a high logic applied to an exclusive-OR gate with the voltage level from the previous interval to determine the signal level in the current time interval.

Kanuma does teach the input data applied to an exclusive-OR gate with the voltage level from the previous time interval to determine the signal level on the bus in the current time interval. [28-1 – 28-N Fig 2; col. 3 lines 37-56].

It would have been obvious to one skilled in the art that the input signals applied to the exclusive-OR gate along with the voltage level from the previous interval may be a high logic level signal. Hence, when applied with the previous voltage level, the signal level of the current time interval may be determined.

15. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanuma [US Pat No. 4,587,445] in view of Buch [US Pat No. 5,230,067].

Kanuma does not explicitly teach the step of maintaining the control signal value at the voltage level from the previous interval when no node drives the bus.

Buch teaches the step of maintaining the control signal value at the voltage level from the previous time interval when no node drives the bus. [col. 5 lines 64-68; col. 6 lines 1-5]

It would have been obvious to one skilled in the art to combine the teachings of Kanuma and Buch in order to avoid a voltage level transition (when no node drives the bus) that would result in increased power dissipation.

16. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanuma [US Pat No. 4,587,445] in view of Albrecht et al [US Pat No. 5,281,822].

Kanuma does not explicitly teach a step of compensating for leakage and cross-coupling effects.

Albrecht teaches a field plate that prevents leakage and cross-coupling. [col. 17 lines 37-40; The field plate compensates for leakage and cross-coupling effects.]

It would have been obvious to one skilled in the art to combine the teachings of Kanuma and Albrecht to compensate for leakage and cross-coupling effects.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pranav Chandrasekhar whose telephone number is 703-305-8647. The examiner can normally be reached on 8:30 a.m.-5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Pranav Chandrasekhar
December 12,2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100